

MULTILEVEL METAL INTERCONNECT  
AND METHOD OF FORMING THE INTERCONNECT  
WITH CAPACITIVE STRUCTURES THAT ADJUST  
THE CAPACITANCE OF THE INTERCONNECT

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BACKGROUND OF THE INVENTION

1. Field of the Invention

10 The present invention relates to multilevel metal interconnects and, more particularly, to a multilevel metal interconnect and method of forming the interconnect with capacitive structures that adjust the capacitance of the interconnect.

15 2. Description of the Related Art

A metal interconnect is a semiconductor structure that electrically connects the individual devices on the semiconductor substrate to realize a desired circuit function. Multiple layers of metal are typically  
20 needed to provide the required interconnections, with current-generation integrated circuits often employing up to seven layers of metal.

FIG. 1 shows a cross-sectional view that illustrates a conventional multilevel metal interconnect 100. As shown in FIG. 1, interconnect 100,  
25 which is formed on a semiconductor substrate 110, has a first layer of isolation material 112 that is formed on substrate 110, and a number of contacts 114 that are formed through isolation layer 112.

In addition, interconnect 100 also has a patterned first metal (metal-1) layer 116 that is formed on isolation layer 112 and contacts  
30 114. Contacts 114 provide an electrical connection with devices formed in substrate 110, such as a source or a drain region of a MOS transistor, while metal-1 layer 116 provides an electrical connection with contacts 114.

In addition, interconnect 100 has a second layer of isolation material 120, known as an intermetal dielectric, that is formed on metal-1 layer 116, and a number of vias 122 that are formed through isolation layer 120. Interconnect 100 also has a patterned second metal (metal-2) layer 124 that is formed on isolation layer 120 and vias 122. Vias 122 provide an electrical connection between patterned metal-1 layer 116 and patterned metal-2 layer 124.

In a similar fashion, interconnect 100 has third and fourth layers of isolation material 130 and 140, respectively. In addition, a number of vias 132 are formed through isolation layer 130 to contact metal-2 layer 124, and a number vias 142 are formed through isolation layer 140.

Further, interconnect 100 has a patterned third (metal-3) layer 134 and a patterned fourth metal (metal-4) layer 144, respectively, that are formed to provide an electrical connection with vias 132 and 142, respectively. A passivation layer 146 is formed on the layer of fourth isolation material 140 and metal-4 layer 144.

Interconnect 100 is conventionally formed, in part, by depositing a first layer of metal on a first layer of isolation material and the contacts formed through the first layer of isolation material. Following this, the first layer of metal is patterned to form the patterned first metal layer. Next, a second layer of isolation material is formed on the patterned first metal layer and the first layer of isolation material.

Vias are then formed through the second layer of isolation material to form an electrical connection with the first layer of metal. A second layer of metal is then deposited on the second layer of isolation material and the vias, and the process continues until all of the required metal layers have been formed.

The layers of isolation material can be implemented with the same or different materials. Silicon dioxide ( $\text{SiO}_2$ ) is commonly used to form each of the isolation layers. Silicon nitride is also commonly used with silicon dioxide, while many current generation processes use dielectric materials with a dielectric constant (K) that is lower than silicon

dioxide.

The layers of isolation material provide electrical isolation between the patterned metal layers as well as between metal lines within a given patterned metal layer. The metal-isolation material-metal  
5 structure forms a parasitic capacitor which has a capacitance that is partially defined by the dielectric constant (K) of the type of isolation material that is used.

Horizontally adjacent metal lines from a patterned metal layer have a line-to-line capacitance that is partially defined by the layer of  
10 isolation material formed between the metal lines. For example, horizontally adjacent metal lines from patterned metal-3 layer 134 have a line-to-line capacitance  $C_a$  that is partially defined by the fourth layer of isolation material 140.

In addition, vertically adjacent metal lines have an interlayer  
15 capacitance that is partially defined by the isolation material between the metal lines. For example, vertically adjacent metal lines from metal-3 and metal-4 layers 134 and 144, respectively, have an interlayer capacitance  $C_b$  that is partially defined by the fourth layer of isolation material 140.

Further, diagonally adjacent metal lines have a cross coupled  
20 capacitance partially defined by the isolation material between the metal lines. For example, diagonally adjacent metal lines from metal-3 and metal-4 layers 134 and 144, respectively, have a cross coupled capacitance  $C_c$  partially defined by the fourth layer of isolation material  
25 140.

One problem with interconnect 100, particularly in sub-micron integrated circuits, is the RC time delay introduced by interconnect 100. The RC time delay, which is dominated by the line-to-line capacitance  $C_a$ , the interlevel capacitance  $C_b$ , and the cross coupled capacitance  $C_c$ ,  
30 significantly impacts the speed of the electrical circuit that is formed on the underlying substrate.

U.S. Patent No. 5,449,953 to Nathanson et al. describe a single level "airbridge" connecting structure for interconnecting monolithic microwave integrated circuits. The manufacturing of these highly specialized structures is, however, not compatible with standard CMOS or bipolar semiconductor device interconnect processing and these structures do not provide a supporting layer beneath the "airbridge."

U.S. Patent No. 6,100,590 to Yegnashankaran et al. describe a multilevel metal interconnect where trenches are utilized to reduce the line-to-line and cross-coupled capacitances  $C_a$  and  $C_c$ . FIG. 2 shows a cross-sectional view that illustrates a prior-art multilevel metal interconnect 200. FIG. 2 illustrates the multilevel metal interconnect taught by U.S. Patent No. 6,100,590.

Interconnect 200 is similar to interconnect 100 and, as a result, utilizes the same reference numerals to designate the structures that are common to both structures. As shown in FIG. 2, interconnect 200 differs from interconnect 100 in that interconnect 200 has a first trench 210 and a second trench 220.

First trench 210 is formed between horizontally adjacent metal lines from the patterned metal-4 layer 144, and through the fourth layer of isolation material 140. In addition, first trench 210 is formed between horizontally adjacent metal lines from the patterned metal-3 layer 134, and through the third layer of isolation material 130.

Second trench 220 is formed between horizontally adjacent metal lines from the patterned metal-4 layer 144, and through the fourth layer of isolation material 140. In addition, second trench 220 is formed between horizontally adjacent metal lines from the patterned metal-3 layer 134, and through the third layer of isolation material 130.

Second trench 220 is further formed between horizontally adjacent metal lines from the patterned metal-2 layer 124, and through the second layer of isolation material 120. In addition, second trench 220 is also formed between horizontally adjacent metal lines from the patterned metal-1 layer 116.

Trenches 210 and 220 are filled with air, which has a dielectric constant of 1.0. Compared with silicon dioxide, which has a dielectric constant of 3.9, the air in trenches 210 and 220 significantly reduces the line-to-line capacitance  $C_a$  and the cross-coupled capacitance  $C_c$ .

5        The contributions of capacitance  $C_a$  and capacitance  $C_c$  to the total interconnect related capacitance depend on the particular geometry of the integrated circuit layout (e.g. metal line-to-line spacing, thickness of the interconnect dielectric material between metal layers, etc.). For conventional microprocessors, for example, capacitance  $C_a$  and capacitance  $C_c$  can account for 60-70% or more of the total  
10        capacitance related to interconnect 100.

      Since the capacitance related to interconnect 100 is the dominant factor affecting the RC time delay in submicron integrated circuits, the presence of trenches 210 and 220 in the interconnect dielectric material  
15        reduces the capacitance related to interconnect 100, thereby increasing device speed.

#### SUMMARY OF THE INVENTION

20        The present invention provides a low capacitance multilevel metal interconnect that allows the capacitance of the structure to be adjusted, and thereby optimized, to respond to signals from devices that are formed on the underlying substrate. In the present invention, the capacitance is adjusted by forming capacitive structures in trenches that  
25        have been formed in the interconnect.

      A multilevel metal interconnect in accordance with the present invention is formed on a semiconductor substrate that has a plurality of active areas. The multilevel metal interconnect includes a plurality of layers of insulation material. The plurality of layers of insulation material  
30        include a first layer of insulation material and a top layer of insulation material. The first layer of insulation material is formed on the semiconductor substrate.

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The interconnect also includes a corresponding plurality of patterned metal layers that are formed on the layers of insulation material so that each patterned metal layer is formed on a corresponding layer of insulation material. The plurality of patterned metal layers includes a first patterned metal layer and a top patterned metal layer, the first patterned metal layer is formed on the first layer of insulation material.

In addition, the interconnect includes a plurality of contacts that are formed through the first layer of insulation material to make electrical connections with the active areas and the first patterned metal layer. The interconnect further includes a plurality of vias formed through the plurality of layers of insulation material other than the first layer of insulation material. The vias make electrical connections with adjacent patterned metal layers.

In accordance with the present invention, the interconnect further includes a capacitive structure that is formed between adjacent metal lines of a patterned metal layer. The capacitive structure is formed from a dielectric material that is different from one of the layers of insulation material.

The present invention also includes a method of forming a multilevel metal interconnect. The interconnect, which is formed on a semiconductor substrate that has a plurality of active areas, includes a plurality of layers of insulation material. The plurality of layers of insulation material include a first layer of insulation material and a top layer of insulation material. The first layer of insulation material is formed on the semiconductor substrate.

The interconnect also includes a corresponding plurality of patterned metal layers that are formed on the layers of insulation material so that each patterned metal layer is formed on a corresponding layer of insulation material. The plurality of patterned metal layers include a first patterned metal layer and a top patterned metal layer. The first patterned metal layer is formed on the first layer

of insulation material.

Further, the interconnect includes a plurality of contacts that are formed through the first layer of insulation material to make electrical connections with the active areas and the first patterned metal layer. In addition, the interconnect includes a plurality of vias that are formed through the plurality of layers of insulation material other than the first layer of insulation material. The vias make electrical connections with adjacent patterned metal layers.

The method comprises the step of etching the layers of insulation material exposed between metal lines in the top patterned metal layer for a predetermined period of time to form a plurality of trenches. Each trench being substantially straight. The method further includes the step of forming a layer of dielectric material in the trenches.

A better understanding of the features and advantages of the present invention will be obtained by reference to the following detailed description and accompanying drawings that set forth an illustrative embodiment in which the principles of the invention are utilized.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross-sectional view illustrating a conventional multilevel metal interconnect 100.

FIG. 2 is a cross-sectional view that illustrates a prior-art multilevel metal interconnect 200.

FIGs. 3A-6A are plan views illustrating a method of forming a multilevel metal interconnect 300 in accordance with the present invention.

FIGs. 3B-6B are cross-sectional views taken along lines 3B-3B to 6B-6B in FIGs. 3A-6A, respectively, in accordance with the present invention.

FIGs. 3C-6C are cross-sectional views taken along lines 3C-3C to 6C-6C in FIGs. 3A-6A, respectively, in accordance with the present

invention.

FIGs. 7A-12A are plan views illustrating a method of forming a metal multilayer interconnect in accordance with a second alternate embodiment of the present invention.

5 FIGs. 7B-12B are cross-sectional drawings taken along lines 7B-7B to 12B-12B shown in FIGs. 7A-12A, respectively.

#### DETAILED DESCRIPTION

10 FIGs. 3A-6A show plan views that illustrate a method of forming a metal multilayer interconnect in accordance with the present invention. FIGs. 3B-6B show cross-sectional drawings taken along lines 3B-3B to 6B-6B shown in FIGs. 3A-6A, respectively. FIGs. 3C-6C show cross-sectional drawings taken along lines 3C-3C to 6C-6C shown in FIGs. 3A-  
15 6A, respectively.

As shown in FIGs. 3A-3C, the method utilizes an interconnect 300 that is conventionally formed on a semiconductor substrate 310. Interconnect 300 includes a first layer of isolation material 312 that is formed on substrate 310, and a number of contacts 314 that are formed  
20 through isolation layer 312. Contacts 314 provide an electrical connection to active regions on the surface of substrate 310. Examples of active regions include the source region of a MOS transistor and collector region of a bipolar transistor.

As further shown in FIGs. 3A-3C, interconnect 300 also includes a  
25 patterned first metal (metal-1) layer 316 that is formed on isolation layer 312 and contacts 314, and a second layer of isolation material 320 that is formed on isolation layer 312 and metal-1 layer 316. Interconnect 300 further includes a number of vias 322 that are formed through isolation layer 320, and a patterned second metal (metal-2) layer 324  
30 that is formed on isolation layer 320 and vias 322. Vias 322 provide an electrical connection between patterned metal-1 layer 316 and patterned metal-2 layer 324.



In addition, interconnect 300 includes a third layer of isolation material 330 that is formed on isolation layer 320 and metal-2 layer 324, and a number of vias 332 that are formed through isolation layer 330. Interconnect 300 further includes a patterned third metal (metal-3) layer 334 that is formed on isolation layer 330 and vias 332, and a fourth layer of isolation material 340 that is formed on the third layer of isolation material 330 and metal-3 layer 334. Isolation layers 312, 320, 330, and 340 can be implemented with, for example, a low-K dielectric.

Interconnect 300 also includes a number of vias 342 that are formed through isolation layer 340, and a patterned fourth metal (metal-4) layer 344 that is formed on isolation layer 340 and vias 342. Vias 332 provide an electrical connection between patterned metal-2 layer 324 and patterned metal-3 layer 334, while vias 342 provide an electrical connection between patterned metal-3 layer 334 and patterned metal-4 layer 344. (Although only four layers of metal are shown, the present invention applies any number of metal layers greater than one.)

The configuration or geometry of the patterned metal layers, such as layer thickness, metal line width, and metal line spacing and pitch, depends on the functionality of the integrated circuit device with which the multilevel metal interconnect will be used. In addition, the process technology used to manufacture the multilevel metal interconnect also effects the geometry of the patterned metal layers.

For example, metal-4 layer 344 can be, for example, as thick as 2 microns, while the remaining patterned metal layers that lie underneath can be, for example, 5000 to 6000 angstroms in thickness. The width of the metal lines for a 0.18-micron process technology can be, for example, 0.28 microns. The thickness of the isolation layers separating one patterned metal layer from the next is dependent upon the process technology used to manufacture the multilevel interconnect, and can be, for example, within the range of 6,000 to 10,000 angstroms.

As shown in FIGs. 3A-3C, the method of the present invention begins by anisotropically etching interconnect 300 for a predetermined

period of time to form a number of trenches TR1-TRs. The anisotropic etch has a high selectivity to metal (i.e. removes interconnect dielectric material at a significantly higher rate than removing metal) to prevent the metal layers from being adversely affected. Trenches TR1-TRs are substantially straight, and adjoin other trenches TR.

The top metal layer, metal-4 layer 344 in this example, functions as a mask for the etching step, with the remaining layers of metal functioning as an etch stop. Thus, depending on the metal patterns in interconnect 300, the bottom surface of a trench TR can have multiple levels, such as trench TR2 (which steps up and over patterned metal-2 layer 324), or a single level such as trench TRs.

The predetermined period of time can be set to any time within a range that has a top end that insures that the etching step does not etch into substrate 310. Following the etching step, interconnect 300 is substantially the same as interconnect 200 shown in FIG. 2. As noted above, interconnect 200 illustrates the multilevel metal interconnect taught by U.S. Patent No. 6,100,590, which is hereby incorporated by reference.

Referring to FIGs. 4A-4C, in accordance with the present invention, a layer of dielectric material 346 is next formed in trenches TR1-TRs. A single type of dielectric material, such as oxide, can be used to fill trenches TR1-TRs, or multiple types of dielectric can be used to fill trenches TR1-TRs (via sequential formation).

In the present invention, dielectric material 346 changes the line-to-line capacitance  $C_a$  and the cross coupled capacitance  $C_c$  of the metal lines in interconnect 300. As a result, the present invention provides a technique for adjusting the capacitance on a metal line to tune interconnect 300 to the operation of the electrical circuit formed on substrate 310.

Referring to FIGs. 5A-5C, following the formation of dielectric material 346, a layer of masking material 350 is formed on the layer of dielectric material 346. Once formed, masking layer 350 is patterned to

protect a capacitor region on the surface of dielectric material 346. Following this, the exposed regions of dielectric layer 346 are anisotropically etched to form one or more capacitive structures 352 and a number of trenches TH1-THp. After the etch, masking layer 350 is  
5 removed, and the method continues with conventional back end processing steps.

Thus, the present invention provides the air dielectric benefits of U.S. Patent No. 6,100,590 to Yegnashankaran et al., plus the additional benefit of selectively adding capacitance to interconnect 300 to tune  
10 interconnect 300 with respect to the electrical circuit formed on the underlying substrate.

In a first alternate embodiment of the present invention, as shown in FIGs. 6A-6C, dielectric material 346 is anisotropically etched for a predetermined period of time prior to the formation of masking layer  
15 350. By utilizing an anisotropic etch prior to forming the masking layer, a capacitive structure 354 with a shorter step height can be formed.

FIGs. 7A-12A show plan views that illustrate a method of forming a metal multilayer interconnect in accordance with a second alternate embodiment of the present invention. FIGs. 7B-12B show cross-  
20 sectional drawings taken along lines 7B-7B to 12B-12B shown in FIGs. 7A-12A, respectively. As shown in FIGs. 7A and 7B, the method utilizes an interconnect 700 that is conventionally formed on a semiconductor substrate 710.

Interconnect 700 includes a first layer of isolation material 712  
25 that is formed on substrate 710, and a number of contacts 714 that are formed through isolation layer 712. Contacts 714 provide an electrical connection to active regions on the surface of substrate 710.

Interconnect 700 also includes a patterned first metal (metal-1) layer 716 that is formed on isolation layer 712 and contacts 714, and a layer  
30 of insulation material 718 that is formed on isolation layer 712 and patterned metal-1 layer 716.

As further shown in FIGs. 7A-7B, the method begins by forming a layer of masking material 720 on insulation layer 718. Once formed, masking layer 720 is patterned to expose a capacitor region on the surface of insulation layer 718. Following this, as shown in FIGs 8A-8B, the exposed region of insulation layer 718 is anisotropically etched to form a first trench 722. (Care must be taken not to etch into substrate 710.) After the etch, masking layer 720 is removed.

Following this, as shown in FIGs. 9A-9B, a layer of dielectric material, such as oxide, is formed on insulation layer 718 to fill up trench 722, and then etched back to form a dielectric region 730 through insulation layer 718. Dielectric region 730 alters the cross-coupled capacitance  $C_c$ . Next, a via mask 732 is formed and patterned on insulation layer 718 and dielectric region 730. Following this, the method continues with conventional steps.

Alternately, as shown in FIGs. 10A-10B, the etching step can be continued for a longer period of time to form a second trench 734. Following the etch, mask 720 is removed. Next, as shown in FIGs. 11A-11B, a layer of dielectric material, such as oxide, is formed on isolation layer 712, insulation layer 718, and patterned metal-1 layer 716 to fill up trench 734. The layer of dielectric material is then etched back to form a dielectric region 736 through insulation layer 718 and between the metal lines of metal-1 layer 716. Dielectric region 736 alters the line-to-line capacitance  $C_a$  and the cross-coupled capacitance  $C_c$ . Following this, a via mask 738 is formed and patterned on insulation layer 718 and dielectric region 736.

After via mask 738 has been formed, the method continues with conventional back end processing steps. Although the method describes the formation of dielectric regions 730 and 736, a number of dielectric regions can be formed between the metal lines of any patterned metal layer.

Further, as shown in FIGs. 12A-12B, when a top patterned metal layer 740 has been formed, the resulting interconnect can be

anisotropically etched for a predetermined period of time that is insufficient to reach region 736 (or 730), or masked to protect region 736 (or 730) and anisotropically etched for a predetermined period of time.

5           Thus, a multilevel, metal interconnect and method of forming the structure according to the present invention have been described. The present invention reduces the capacitance related to the interconnect of any CMOS, BiCMOS, or bipolar integrated circuit that includes a multilevel metal interconnect by eliminating a portion of the interconnect  
10       dielectric material therein, thereby decreasing the line-to-line capacitance  $C_a$  and the cross coupled  $C_c$  capacitance components. In addition, the present invention allows capacitance to be selectively added to tune interconnect 300 with respect to the electrical circuit formed on the underlying substrate.

15           It should be understood that various alternatives to the embodiments of the invention described herein may be employed in practicing the invention. For example, the present invention applies equally to a dual damascene process. It is intended that the following claims define the scope of the invention and that structures and  
20       methods within the scope of these claims and their equivalents be covered thereby.

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